**Instruction Fetch Unit (Finite State Machine for implementing**

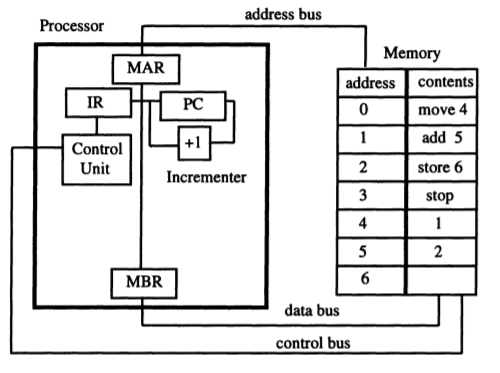
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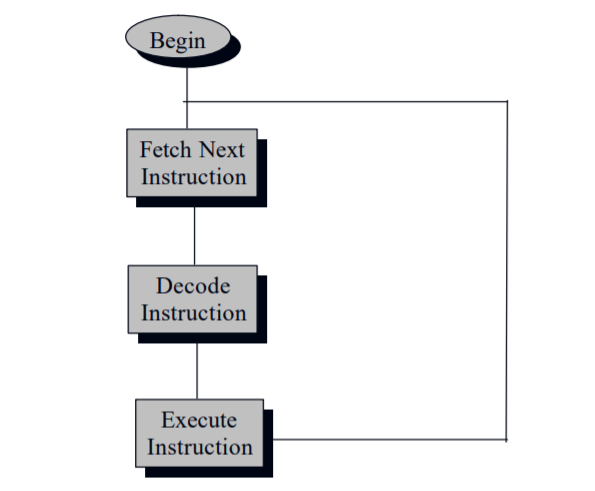
The instruction unit (IU), also called instruction fetch unit (IFU) or instruction issue unit (ISU), in a central processing unit (CPU) is responsible for organising program instructions to be fetched from memory, and executed, in an appropriate order. It is a part of the control unit, which in turn is part of the CPU. In a Microcomputer system the processor is connected to main memory by **a data, address** and **control bus** as shown in figure 1 below. A program consists series of instructions or actions to be carried out by the processor. These actions are performed on data, Instructions and data are stored in primary or memory during program execution. In figure 1, instructions and data occupy various memory locations, each location being identified by a unique address. When running a program, the processor fetches the instructions by providing an address on the address bus and reading instruction from the data bus and to carry out this task, the processor uses a number of internal registers, basically registers is a small high-speed memory location used for temporary storage of data or control information. There are four registers **Memory Address Register** (MAR) holds the address of the current instruction that is to be fetched from memory, or the address in memory; a **Memory Buffered Register** (MBR) either of data read from memory or data retrieved from memory an **Instruction Register** (IR) is the part of a CPU'S Control Unit that holds the instruction currently being executed or decoded. **Memory Data Register** (MDR) which hold the store data being reference and **Program Counter** (PC) in the computer processor which has the address of the next instruction to be executed from memory. It is a digital counter needed for faster execution of tasks as well as for tracking the current execution point. These registers are connected together by an internal data path or bus. The flow of data along the bus is managed by the Control Unit (CU) It tells the computer's memory, arithmetic and logic unit and input and output devices how to respond to the instructions that have been sent to the processor. The **Decode cycle** is used for interpreting the instruction that was fetched in the Fetch Cycle. The operands are retrieved from the addresses if the need be. **Execute Cycle** This cycle as the name suggests, simply executes the instruction that was fetched and decoded. **Interrupt Cycle** An interrupt can occur any time during the program execution. Whenever it is caused, a series of events take place so that the instruction fetch execute cycle can again resume after the OS calls the routine to handle the interrupt.

**SUMMARY**:

Programs are executed by repeatedly fetching instructions from Memory in to the processor and then executing them. This is called the fetch-execute cycle. Three buses are used to exchange information with the Memory Unit: An Address Bus, a Data Bus and a Control Bus. To organise this flow of instructions, the processor uses a number of special purpose registers: a Program Counter, an Instruction Register, a Memory Address Register and a Memory Buffer Register. Instruction decoding is performed by the Control Unit, which generates appropriate control signals in response to the opcode of the instruction. The operand field is used to specify the address of any data required by the instruction. An ALU is used to carry out arithmetic and logic operations on data, temporarily stored in a Data Register or passed to it from the MBR. A Condition Code Register is used to record details about the result of the operation.



**Figure:1**



**Figure: 2 Basic Instruction Fetch Execute Cycle**